FRS-HD-CHO / FRS-HD-CHO-ASI / ASI-CHO-2x1-PB

HD/SD-SDI 2x1 Change-Over
with Frame Synchronizer
and/or
ASI 2x1 Change-Over

User manual

Rev. K

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Revision history

Current revision of this document is the uppermost in the table below.

Rev.	Repl.	Date	Sign	Change description
K	9	2015-05-14	MB	Cover page update; DoC removed; no other changes to content
9	8	2012-08-10	TB	Corrected DIP switch description for ASI-CHO-2x1. Added min/max audio delay.
8	7	2012-05-04	TB	Corrected table 2, Connections. Added description of the GPIO mode selector under GPI alarms.
7	6	2012-02-22	TB	Added the ASI-only variant, ASI-CHO-2x1-PB. Updated several screen-shots to current look (Multicon 3.6.0)
6	5	2011-08-15	TB	Added clarification about –ASI upgrade and HW versions.
5	4	2011-05-19	TB	Added description for the ASI variant. Some changes to DIPs and the list of commands. Added Declaration of Conformity.
4	3	2010-02-24	TB	Added APVF and silence trigger (ch.5.2), updated block diagram (ch.1.1), replaced ‘kill’ with ‘mute’ as audio fallback (ch.5.13), replaced misleading figures on sync (ch.5.4.1).
3	2	2009-05-12	RS	Corrected cable equalization spec on inputs
2	1	2009-05-06	SHH	Added a requirement of termination of unused SDI-inputs/outputs in chapter 3.3.
1	0	2009-03-03	SHH	Updated document with Label generator and corrected an error in the mtx 0 description
0	B	2008-12-15	NBS	First release of product.
B	A	2008-12-04	SHH	Re-written and new Gyda features included.
A	-	2008-10-17	SHH	Initial release.

Contents

1 Product overview

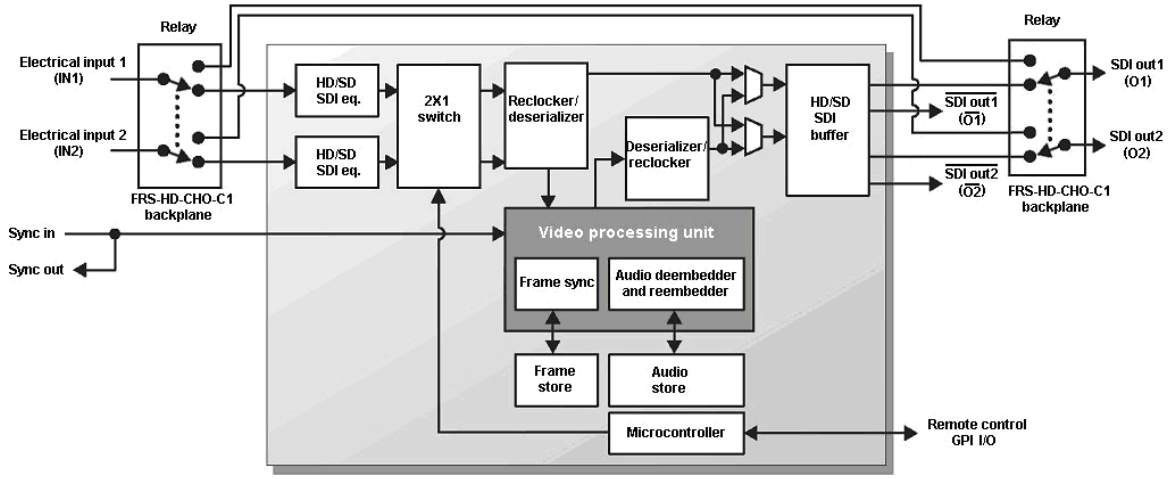


Figure 1: Simplified block diagram of the FRS-HD-CHO card

1.1 Product description

The base version of the Flashlink FRS-HD-CHO is a 2x1 HD/SD change-over module with a frame synchronizer that can lock an HD-SDI or SD-SDI input to a black & burst or tri-level reference signal. A de-glitcher ensures an always error-free output.

The change-over functionality covers numerous switching criteria that analyses video and audio integrity and content. The switching criteria are placed into several logical groups, each of which can have their own timing.

The FRS-HD-CHO has an extensive audio functionality, including audio cross point matrix, channel swapping, relative audio delay, and audio gain. The module is also well suited for Dolby-E.

An extension - and even a separate version - exists that will also handle change-over switching on ASI inputs, but then without the frame synchronizer, de-glitcher, and audio functionality.

The user parameters of the card can either be changed by switches on the board, or by the Multicon Gyda system controller.

1.1.1 Product versions

This product comes in three versions: The base model FRS-HD-CHO for HD/SD-SDI, the FRS-HD-CHO-ASI with a selectable SDI or ASI mode, and an ASI-only version called ASI-CHO-2x1-PB.

The ASI-CHO-2x1-PB is not designed to be upgradable to an FRS-HD-CHO or an FRS-HD-CHO-ASI. The user interface for ASI-only is however much reduced compared to the SDI capable versions with frame synchronizer and audio embedding/de-embedding, making the ASI-CHO-2x1-PB very easy to understand, set up, and use.

Some FRS-HD-CHO modules can be upgraded to FRS-HD-CHO-ASI with a software key (for a nominal fee). These modules can be recognized by the way they respond to a '?' command on the serial communication bus, and the way they present themselves in the Multicon Gyda configuration page. If the reply to the '?' command contains a line that says "Serial rev 1728201000000001" (the actual 16-digit number will be different) *and* a line that says "HW rev 1.1", or there are two lines at the very bottom of the Multicon configuration page that looks like below, the module can be upgraded to the -ASI version with a software key:

HW	1.1
Serial	1728201000000001

If one (or both) of these two lines is not present, or the HW version is reported as 1.0, or the serial number reported is “XXXXXXXXXXXXXXX” (literally sixteen X characters), the module cannot be field upgraded from the FRS-HD-CHO to the FRS-HD-CHO-ASI version. Of course, the module can still be upgraded with the latest firmware and continue to work as an FRS-HD-CHO.

1.1.2 Key features

- Passive bypass from both inputs to non-inverted outputs with less than 25m loss of cable length (enables full redundancy, see app. note in appendix)
- HD/SD video support, including DVB-ASI in through mode
- Separate ASI mode available (as an upgrade from the ‘normal’ FRS-HD-CHO)
- Separate ASI-only version available with a much simplified user interface
- De-glitching of input video signal (always seamless output)
- Intelligent change-over functionality with switching criteria:
  - Video integrity check
  - Audio integrity check
  - Video freeze detect (full frame or active area)
  - Video black detect (with adjustable black threshold)
  - Time code freeze
  - Audio silence detect (with adjustable silence threshold)
- Latched switching
  - Ripple rejection latching with adjustable hold times
  - Switching between inputs on switching line
  - GPI inputs for external control of switch
  - Individual detection timings for video signal integrity, audio signal integrity, video content and audio content.
- HD/SD frame sync/delay (8 frames max)
- luma/chroma gain and level adjustment
- Audio delay enabling Dolby-E processing delay correction
- Audio router for embedded audio
- Embedded audio gain adjustment
- Audio fade out/fade in at switching or frame-wrap
- SDI Label inserter
- EDH processing

2 Specifications

Electrical SDI input

Number of inputs	2
Connectors	75 Ohm BNC
Equalization	Automatic; >300m @270Mbps w/Belden 8281, with BER < 10E-12 >130m @1485Mbps w/Belden 1694A, with BER < 10E-12
Input Return loss Active input	>15dB, 5MHz -1.485GHz
Input Return loss passive bypass	>15dB, 5MHz -742.5MHz >10dB, 742.5MHz - 1.485GHz
Jitter tolerance	SD limit: 10Hz-1kHz: >1 UI 10kHz – 5MHz: >0.2 UI HD limit: 10Hz-100kHz: >1 UI 100kHz–10MHz: >0.2 UI

Electrical Sync input

Connector	75 Ohm BNC
Format	Black & Burst, Tri-level
Input Return loss	>35dB @ < 10MHz, 30dB @ < 30MHz

Electrical SDI outputs

Number of outputs	4
Connectors	75 Ohm BNC
Return Loss O1, O2 Active output	>15dB, 5MHz -1.485GHz
Output Return loss O1, O2 Passive bypass	>15dB, 5MHz -742.5MHz >10dB, 742.5MHz - 1.485GHz
Return loss !O1, !O2	>15dB, 5MHz -742.5MHz >10dB, 742.5MHz - 1.485GHz
Output signal level	800mV +/- 10%
Output signal rise / fall time 20% - 80%	SD limit: [0.4ns – 1.5ns]; <0.5ns rise/fall var. HD limit: < 270ps, <100ps rise/fall var.
Amplitude overshoot	<10%
Output timing jitter	SD: <0.2 UI HD: <1 UI
Output alignment jitter	SD: <0.15 UI HD: <0.2 UI

Supported standards

SD, 270 Mbps	SMPTE 259M, SMPTE 272M-AC
HD, 1485 Mbps	SMPTE 292M, SMPTE 274M, SMPTE 291M, SMPTE 296M, SMPTE 299M
DVB-ASI[1]	50083-9, error detection according to ETR290 1.1 and 1.2
Video switch point definition and sync	SMPTE RP168 (tri-level), SMPTE 170m, ITU-R. BT.470
EDH	Compliant to SMPTE-RP165
Video Payload Identification	SMPTE 352M-2002

Other

Power consumption	3.5W @ 5V 1.2W @ 15V

[1] The ASI support can be purchased as an optional upgrade.

3 Configuration

The board can be configured both manually and through the system controller Multicon Gyda. However, only a few of the configurable parameters are available when operating in manual mode.

3.1 Manual mode

To reach manual mode DIP16, labeled OVR, on the board must be switched on (to the right) and the board must be re-booted. This takes the board out of Multicon Gyda control (if it was previously set to off) and a number of the module's features will be controlled directly by the other DIP switches, the rotary switch, and the two pushbuttons. Settings not controlled by any of these switches are kept unchanged from previous session (factory setup or Gyda setup).

The Manual Mode configuration controls are all found on the front side of the board. There are two sets of DIP switches, one rotary switch and two push buttons. The slide switch on the lower right is used to select sync source for both modes of operation, see 3.1.2 below.

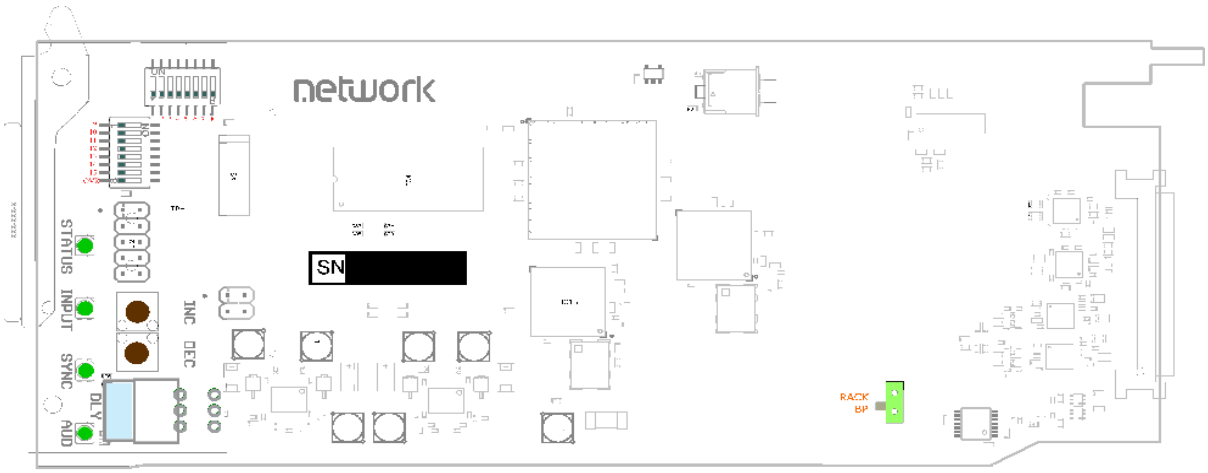


Figure 2: The figure shows a top view component printout of the board. LEDs, push-buttons, the rotary switch and the 2 sets of DIP-switches are colorized.

3.1.1 Rotary switch and push buttons

The *rotary switch*, labeled DLY, adjusts the *phase delay* by -5 to +4 video lines. It is only functional when a sync signal, black & burst or tri-level, is present at the sync input. The rotary switch is accessible from the front of the rack.

The *push buttons,* labeled INC and DEC, are used to fine adjust the *phase delay* by samples. It can adjust within +/- ½ video line for the video standard seen by the module.

3.1.2 Slide switch

The slide switch on the lower right side of the card selects between backplane sync input (BP) and Flashlink rack distributed sync (RACK). The rack distributed sync is a future feature upgrade of the Flashlink frame, and at present the switch should always be set to its lower position (to BP).

3.1.3 Factory reset function

The factory reset function restores the module to its default settings. These settings are just a start condition for the board, and changes done by the user will still take effect and be stored.

The factory reset is initiated by setting DIPs 15 and 16 to the 'On' position and booting the module. All inputs signals should be removed. The status LED will stay permanently orange, and the module will not complete its start-up. DIP 15 should then be returned to the 'Off' position, while DIP 16 should be set to the desired mode of operation before the module is booted again. This starts the actual internal reset process, and the module should now be left powered for at least 10 seconds or the complete set of default setting may not be stored properly. If necessary, the reset operation can be performed multiple times.

3.1.4 DIP switch functions

The two sets of DIP switches are labeled with a number running from 1 to 15. The 16th DIP is labeled *OVR.*

> Note that the left DIP switch of the horizontal DIP package is number 1. The top DIP switch of the vertical DIP package is number 9.

Switch #	Function name	Function DIPs	Comment
1	ASI/SDI input mode (FRS-HD-CHO-ASI only)	Off: input is SDI On: input is ASI (For valid ASI output, DIP12 and/or DIP13 must also be set to the 'Through position')	FRS-HD-CHO-ASI only. Note: Firmware older than ver. 1.10 use this DIP for a latch on/off input setting.
2	CHO priority	Off = In1 On = In2	
3	---	Reserved	Note: Firmware older than ver. 1.10 use this DIP for selection between Loss Of Signal and Loss Of Lock.
4-5	Lock & Hold time	DIP[5 6] = [Off Off] => Minimum DIP[5 6] = [Off On] => 1s DIP[5 6] = [On Off] => 4s DIP[5 6] = [On On] => Reserved	Only valid if latch is on
6	Audio gen	Off = 1kHz Sine On = Black sound	
7	Emb. enable	Off: No audio embedded On: Audio embedded	When off, the audio is left un-touched on the SDI stream. When on, the audio configured to be embedded is embedded into the SDI.
8	GPIO setup	Off: SDI-CHO-2x1 mode On: FRS-HD-SDI mode	See the GPI input output description below.
9 - 11	Frame delay	DIP[9 10 11] = [Off Off Off] => 0 frms DIP[9 10 11] = [Off Off On] => 1 frms DIP[9 10 11] = [Off On Off] => 2 frms DIP[9 10 11] = [Off On On] => 3 frms DIP[9 10 11] = [On Off Off] => 4 frms DIP[9 10 11] = [On Off On] => 5 frms DIP[9 10 11] = [On On Off] => 6 frms DIP[9 10 11] = [On On On] => 7 frms	With a sync-input present, this sets the minimum frames delay. Without a sync-input present this sets the no. of frames delay relative to the input.

Switch #	Function name	Function DIPs	Comment
12	SDI OUT 1	Off: through mode On: processed mode	In through mode the video only goes through a re-clocker.
13	SDI OUT 2	Off: through mode On: processed mode	In through mode the video only goes through a re-clocker.
14	Video Generator	Off: Color bar On: Black field	This is the video generator signal that is shown when video is detected lost according to the fallback rule set in GYDA.
15	RESET	Off: Use values preset by GYDA. On: RESET to factory defaults	To reset, both DIP 15 and DIP16 must be set on before powering on. DIP 15 and 16 is read at power up. The reset is not done until DIP 15 is set back to off and re-powered.
16	OVR	Off: GYDA mode On: Manual mode	This DIP is only read at power up. OVR is short term for GYDA override

Table 1: DIP SWITCH FUNCTIONS

For the ASI-CHO-2x1-PB, only DIPs number 2, 4, 5, and 8 (and 15+16) will have any effect. The rest will be ignored and can be set to any position.

3.2 Gyda mode

All functions of the card can be controlled by the Multicon Gyda control system. In Multicon Gyda the module has an information page and a configuration page.

3.2.1 Information page

The information page for ASI-CHO-2x1-PB is a subset of the information page for FRS-HD-CHO, which in turn is a subset of the information page for FRS-HD-CHO-ASI. While the FRS-HD-CHO and FRS-HD-CHO-ASI only differ in that the latter has an extra line for “Input signal type”, the ASI-CHO-2x1-PB information page is quite reduced, because the frame synchronizer and audio embedder/d-embedder functionality quite simply isn’t included. The difference between Figure 3 and Figure 4 should make this clear. The following paragraphs will describe the information page for FRS-HD-CHO(-ASI), but as far the mentioned items are also present in the ASI-CHO-2x1-PB information page, the description will apply for that product version as well.

The information page shows a dynamic block-diagram of the board and some additional information in textual form. The block diagram updates with the boards status, showing input signal selected, signals missing (by red crosses over signal lines), and routing through switches. It also shows the audio matrix selections that have been made on the configuration page.

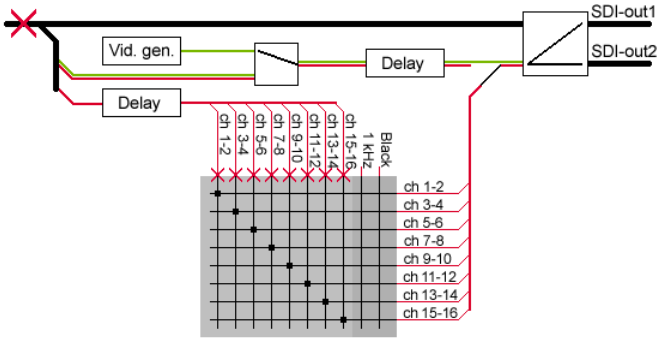
Note that if embedded audio is missing from a group, the user will still be allowed to select those inputs in the matrix, but the output will go to a fallback position. Missing audio channels will be shown in the block diagram with a red cross over the matrix input line.

The text on the information page gives information about functionality not displayed on the dynamic block diagram.

The *video delay* represents the actual delay between input and output video.

If the ASI option has been purchased, the name of the module will have '-ASI' appended. In addition, a line 'Input signal type' followed by 'SDI' or 'ASI' will appear as a reminder of the selected mode, ASI or SDI.

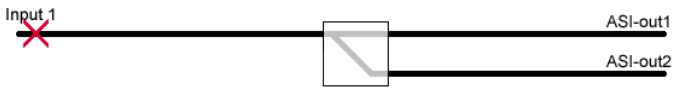
FRS-HD-CHO-ASI



Input signal type	SDI						
Phase delay	0 samples						
Electrical input 1	Loss of signal						
Electrical input 2	Loss of signal						
Reclocker	Loss of lock						
Sync source	Missing						
Video delay	0 ns			0 samples			
Relative audio delay	0 samples						
Signal integrity	1080/25i		Error counter: 0		Reset		
			NO_EDH	VS	FF-CRC	AP-CRC	LOCK
	CCS	YCS	CCRC	YCRC	LNUM	SAV	EAV

Figure 3: Gyda information page for FRS-HD-CHO-ASI

ASI-CHO-2x1-PB



Electrical input 1	Loss of signal
Electrical input 2	Loss of signal
Reclocker	Loss of lock

Figure 4: Gyda information page for ASI-CHO-2x1-PB

3.2.2 Configuration page

The different configuration possibilities are explained in detail in Chapter 5, under the corresponding functions.

3.3 Connections

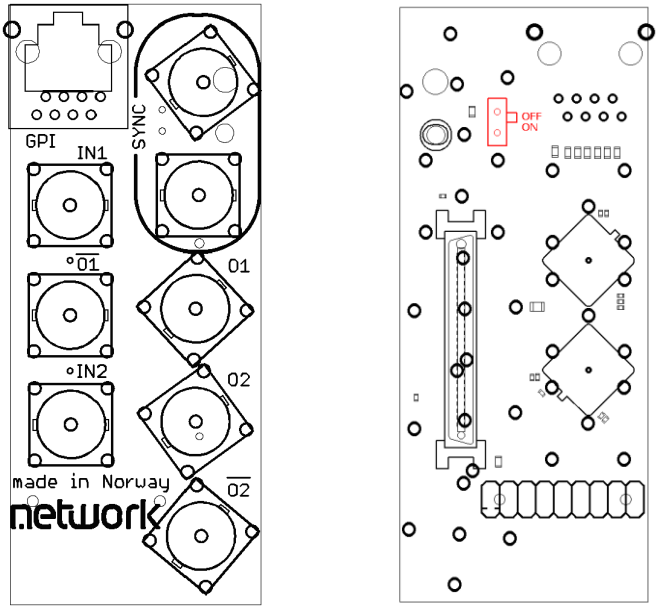


Figure 5: FRS-HD-CHO-C1 backplane
right: connection side left: component side

The backplane for the FRS-HD-CHO is labeled FRS-HD-CHO-C1. The table below shows the connectors and their functions.

Function	Label	Connector type
HD/SD-SDI or ASI input 1	IN1	BNC
HD/SD-SDI or ASI input 2	IN2	BNC
HD/SD-SDI or ASI output 1	O1	BNC
HD/SD-SDI output 1, inverted (ASI is a polarized signal, i.e. the inverted signal is not valid ASI unless inverted a second time)	$\overline{O1}$	BNC
HD/SD-SDI or ASI output 2	O2	BNC
HD/SD-SDI output 2, inverted (ASI is a polarized signal, i.e. the inverted signal is not valid ASI unless inverted a second time)	$\overline{O2}$	BNC
Black & Burst/ tri-level input	SYNC	BNC
Black & Burst/ tri-level input	SYNC	BNC
GPI in	GPI	TP45, pin 5 & 6
GPI out	GPI	TP45 pin 1, 2, 3, 4, 7 (pin 8 = GND)

Table 2: Connector functions

Unused SDI/ASI-inputs/outputs must be terminated with 75 Ohm.

3.4 Sync input

The two sync inputs on the backplane are internally connected. It is possible to use one as input and the other as a looped output. The backplane also features a switchable termination. By setting the “red” switch in the upper right of Figure 5 to the ‘On’ position the sync input will be terminated to 75 Ohms.

4 Operation

4.1 Front panel LED indicators

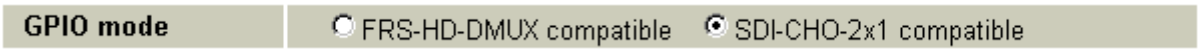
Diode \ state	Red LED	Orange LED	Green LED	No light
Card status	PTC fuse has been triggered or FPGA programming has failed	Module has not been programmed, RESET and OVR DIPS are on or module is updating firmware.	Module is OK	Module has no power
SDI input status	Video signal absent.	Video signal present but card not able to lock VCXO	Video input signal in lock	Module has not been programmed
Sync input status	Sync signal absent	Sync signal present but card unable to lock VCXO	B&B or Tri-level sync in lock	Module has not been programmed
Audio input status	No audio embedded in incoming video	One, two or three audio groups embedded in incoming video	4 audio groups embedded in incoming video	Module has not been programmed

A few special conditions exist for the LEDs:

- When upgrading the module's FPGA software there a transfer stage followed by an unpacking stage. During the unpacking the LEDs will display a running-lights pattern, three orange LEDs and one unlit LED.
- When running a Locate command all four LEDs will flash slowly between orange and unlit.
- When running the module in manual mode the two push buttons can be used to set the sample part of the phase delay. When the end of the adjustment range is reached, the closest LED will flicker briefly. Returning to 0 samples by pressing both push buttons simultaneously will be acknowledged by the two middle LEDs flickering briefly.

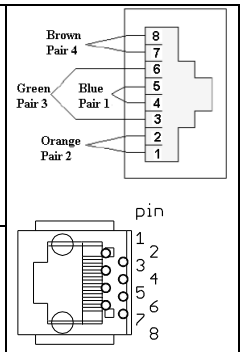
4.2 GPI alarms

The FRS-HD-CHO can have the GPI outputs to be setup as "change-over style" or "frame sync style", either by DIP8 or by Multicon Gyda control. In the graphical user interface of Multicon Gyda, the selector looks like this:



The selection "FRS-HD-DMUX compatible" is equal to what the table on the next page refers to as "frame-synch style", while "SDI-CHO-2x1 compatible" is equal to the "change-over style" of the GPIO lines. As the table on the next page shows, the difference lies in the behavior of pins 3, 4, and 7.

4.2.1 Functions of 8pin modular jack

GPI name (change-over style / frame-synch style)	Function (change-over style / frame-synch style)	Pin #	Mode	Direction	
Status	General error status for the module.	Pin 1	Inverted Open Collector (open is alarm)	Output	
LOS[2]	Loss of signal or lock at selected input	Pin 2	Open Collector	Output	
Input 1/ Sync loss	Input 1 selected (IN1)/ Sync input loss of signal or lock	Pin 3	Open Collector	Output	
Input 2/ Framedelay[2]	Input 2 selected (IN2)/ Outputs a pulse with length equal to frame delay	Pin 4	Open Collector	Output	
Reset	Reset selected input to main	Pin 5	TTL, 0V = active level	Input	
Set	Set selected input to standby	Pin 6	TTL, 0V = active level	Input	
Input 2/ Frame delay[3]	Connected to pin 4 on backplane	Pin 7	Open Collector	output	
Ground	0 volt pin	Pin 8	0V.		

[2] EDH errors will not be shown at GPI output.
[3] Pin 4 and 7 are connected on TP45 connector to be compatible with both FRS-HD-SDI and SDI-CHO-2x1.

5 Functional description

5.1 Selection of input signal type (FRS-HD-CHO-ASI only)

If the optional ASI upgrade has been purchased, the top of the configuration page will be a selector between SDI input mode and ASI input mode. In ASI mode, the module will not lock to a non-ASI SDI signal. The ASI signal will not pass *through* the FPGA, it will only be passed *to* the FPGA, enabling the FPGA to look for valid ASI data.

> In order to get an output in ASI mode, the video output must also be taken from the Pass-through position (see 5.10, Video output selection), meaning that the video output is re-clocked only.

Figure 6: Gyda view of the input signal type selector

5.2 SDI data path

HD/SD-SDI input is selected from input 1 or 2, equalized, re-clocked and transferred to a processing unit. Here the signal is first sent through a *de-glitcher* that cleans up errors that might appear on input signal, for instance due to switching. After the de-glitcher the parallel video is split in two paths, one going directly to a *frame-store buffer*, the other sent to the *audio de-embedder*.

The 16 audio channels coming from the de-embedder are bundled **in pairs** and sent to an audio store buffer (being the same as the frame store buffer). The audio is fetched from the audio store buffer according to a user specified delay and sent to an *Audio Cross Point.* The output of the Audio Cross Point can be any pair of audio channels de-embedded from the incoming video stream, an internal 1 kHz sine or an internal “black sound”. “Black sound” is in function mute, but it produces a waveform pattern which is different from mute. Each channel pair from the cross point outputs enters an A*udio Processing Block*, where the paired channels may be level adjusted and shuffled. After the audio processing block the audio enters the *Audio Embedder*.

The video (with audio still inserted) is fetched from the frame buffer with the user specified delay and sent to a *Video processing block* (gain, offset and hard clip legalizing), followed by an *EDH processing block*. After the EDH block the video and audio is embedded according to the user settings and the video is sent from the processing unit to a re-clocker. Here the signal is converted back to SDI and sent to a 2x2 output switch.

The buffered output switch is a 2x2 cross point switching between an equalized and re-clocked input (through) and a video processed input (processed). The two outputs are sent to two paired (non-inverting and inverting) outputs.

5.3 Video input selection

The FRS-HD-CHO has two electrical inputs. The input can be chosen either by an automatic selection with priorities and rule of switching, or by manual selection. If there is a sync input connected, the board will switch the signals on the switching line of the present format.

Manual selection mode

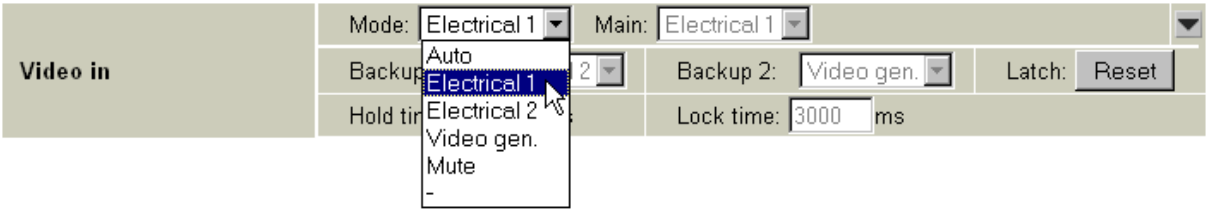


Figure 7: Gyda view of input 1 selected in manual mode.

Automatic selection mode

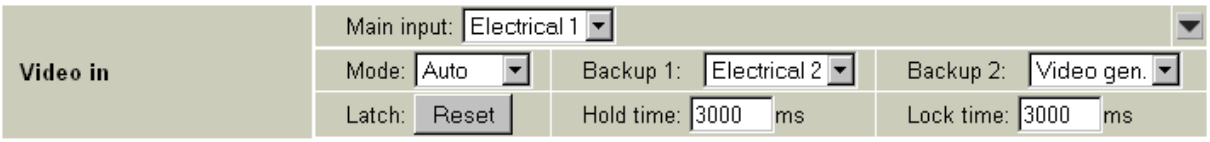


Figure 8: Gyda view of the input selection

If in Gyda the *video in mode* choice is set to auto, three input choices can be made for three priorities; electrical 1, electrical 2 or mute/generator[4]. When signal is missing on one priority, the change-over will switch to the next priority and look for signal. If only two priorities are needed, i.e. one main and a fallback, the third priority can be disabled by setting it to '–'.

> Note that the ASI-CHO-2x1-PB product version does not have the *Video gen.* and *Mute* choices. Because no version of the FRS-HD-CHO has a built-in ASI generator, no fallback is available when using ASI input signals. This is also true for the FRS-HD-CHO-ASI; Even though the *Video gen.* and *Mute* choices are available regardless of the selected mode (SDI or ASI), no actual fallback will be available for lost ASI sources.

Hold time and lock time controls how long a signal can be missing before the next priority is used, and how long a signal has to be present before it is considered to be OK again. This module is always latching, which means that is doesn't switch from a fallback back to the main input unless it is either ordered to do so (the latch reset button), or if the fallback signal also disappears.

Triggers

In addition to the loss of signal and lock detect, there are a set of *triggers* that can force the switching to next priority. Equal types of triggers are grouped together in a trigger block. A trigger block consists of a *switching enable* signal, a *trigger selection mask*, a *Boolean operator*, a *hold time* and a *threshold*.

The trigger block always report status of all triggers inside the trigger block.

The switching enable signal (enable/disable radio button) enables the trigger to do a switch between the inputs after detecting a continuously present error over a *hold time*.

The trigger selection mask selects which detections are enabled to do switching.

The Boolean operator is either "*and"* or "*or"*. It controls whether the switching should be based on either (*or*) or all (and) of the selected triggers in the trigger selection mask.

The trigger to switch time is the time that a trigger must be continuously present before a switching of the inputs will happen.

[4] The processed video out block selects whether the output goes to mute or generator at loss of signal

Level is number to set a threshold for a content check. The format of the levels will differ between trigger blocks. Not all trigger blocks have a threshold.

The trigger blocks for the FRS-HD-CHO are:

- video error trigger block
- video content trigger block
- audio error trigger block 1 - 4
- audio in silence trigger
- audio out clipping trigger
- active picture video freeze and silence trigger

The different trigger blocks with their respective trigger masks are shown in Figure 9.

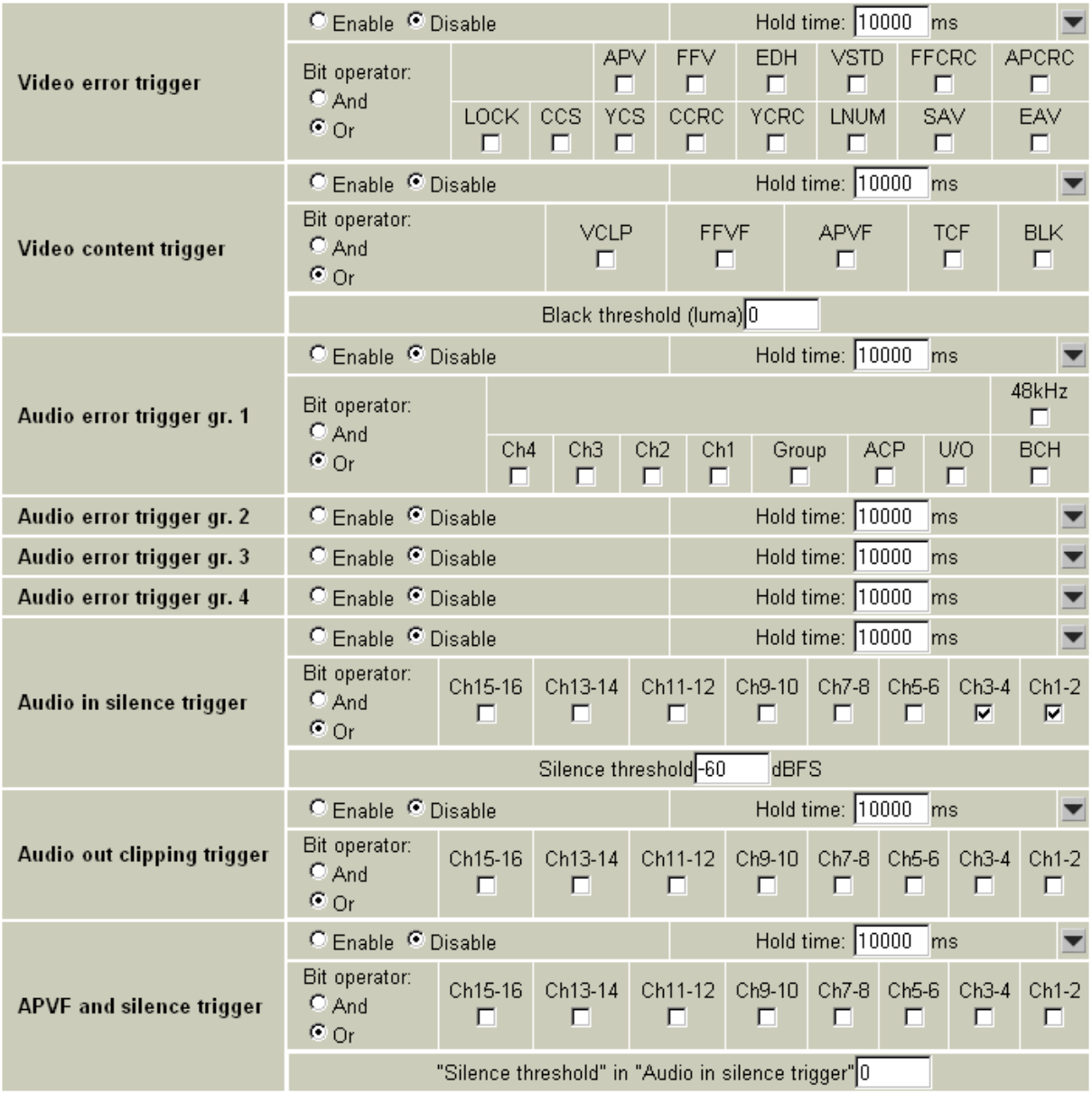


Figure 9: The available triggers and their masks.

Term	Description
Video error trigger	
APV	Active picture CRC invalid
FFV	Full frame CRC invalid
EDH	EDH package missing (SD only)
VSTD	Video standard error
FFCRC	Full frame CRC error (SD only)
APCRC	Active picture CRC error (SD only)
LOCK	Loss of re-clocker lock
CCS	Chroma checksum error
YCS	Luma checksum error
CCRC	Chroma CRC (HD only)
YCRC	Luma CRC (HD only)
LNUM	Line numbering error (HD only)
SAV	Start of active video error
EAV	End of active video error
Video content trigger	
VCLP	Video clipping detected by legalizer
FFVF	Full frame video freeze detected
APVF	Active picture video freeze detected
TCF	Time code freeze detected
BLK	Black video detected (below set threshold)

Term	Description
Audio error trigger group 1 - 4	
Ch 1 (2,3,4..)	Channel 1 set inactive in audio control package
Group	Audio group missing (in audio trigger 1,2,3,4, group = group 1,2,3,4)
ACP	Audio control package missing
U/O	Audio underflow/ overflow ch. 1 - 4
BCH	Audio CRC error
48kHz	Sampling rate different from 48kHz detected
Audio in silence trigger	
Ch1-2 (3-4..15-16)	Audio level received in channel 1 and 2 below set silence threshold
Audio out clipping trigger	
Ch1-2 (3-4..15-16)	Audio out (after audio processing gain) is clipped.
APVF and silence trigger	
Ch1-2 (3-4..15-16)	Audio level received in channel 1 and 2 below set silence threshold while active picture video freeze is also detected

The black detect threshold is an integer between 0 and 255. Selecting a threshold of 10 will accept everything below 74 (04Ah) luma and between +10 and -10 (1F6h and 206h) chroma as black.

The silence threshold can be adjusted in 6dB steps from -90dB to -18dB.

> ‘Audio in silence trigger’ and ‘APVF and silence trigger’ share the same silence threshold setting. It can only be adjusted from the ‘Audio in silence trigger’. The threshold value in ‘APVF and silence trigger’ will always display as 0 and the threshold value in ‘Audio in silence trigger’ is always the one used by the module.

5.4 De-glitcher

The de-glitcher corrects timing errors within a line. The de-glitcher has a 2048 samples buffer. When the first signal is present, we call it the “initial phase signal”, data is taken from the centre of this buffer. If the timing reference of the video signal changes, when for instance a new source being switched into the signal path, the timing errors occurring by this change will be corrected if the new timing reference is within +/-1024 samples of the “initial phase signal”. This also goes for all consecutive timing references.

If a signal is more than +/-1024 samples off relative to the “initial phase signal”, the output will repeat the last frame, refill the 2048 samples buffer and take out data from the centre of the buffer. This new signal is now considered the “initial phase signal”. Audio will fade out when a frame repeat is being done, and fade in at the new frame.

Hence, it produces an error free video output without frame wrapping when the video input comes from a router with synchronous input video signals that all lies within +/-1024 samples of each other.

> The de-glitcher output is always seamless. When a signal is repeated the audio is faded out. It fades in at the new frame.

5.5 Frame synchronizer

The frame synchronizer consists of a frame store buffer and some control logic. The frame store buffer can store up to 8 full HD frames. Data is fetched from this buffer according to the user settings by force of the control logic. The control logic sets the frame synchronizer into different modes dependent on the presence of a sync input.

5.5.1 Frame sync mode

If a sync input (B&B or Tri-level) is present, the frame synchronizer will output a signal that has a delay relative to this signal. Two parameters can be set; "**Phase delay**" and "**Video delay**".

Phase delay	0	lines	0	samples	
Video delay	2	frames	0	lines	0 samples

Figure 10: Gyda view of the video delay settings

Let us first focus on the *phase delay*, which also may be called “output phase delay”. This parameter can be positive or negative, and determines the relationship between the outgoing video and the sync signal. The parameter really determines a delay on an internal sync signal, isync[5]. The output is synchronous with isync, see Figure 11.

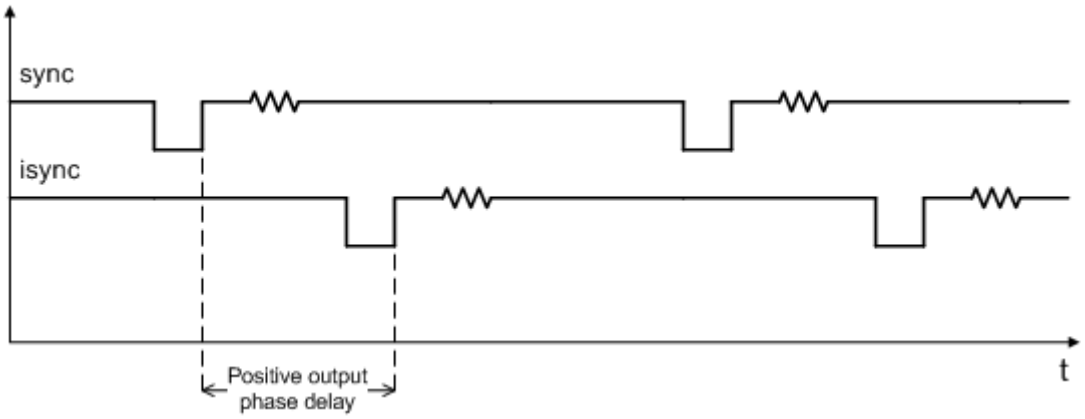


Figure 11: Positive phase delay

Figure 11 show how the sync signal and the isync signal would look on an oscilloscope, if converted to analogue signals. The delay of isync can be given in frames, lines, and samples. The delay can be negative, see Figure 12.

[5] Note that *isync* is not a physical entity, but a term used in this context to explain the delay process and the use of the configurable parameters related to this process.

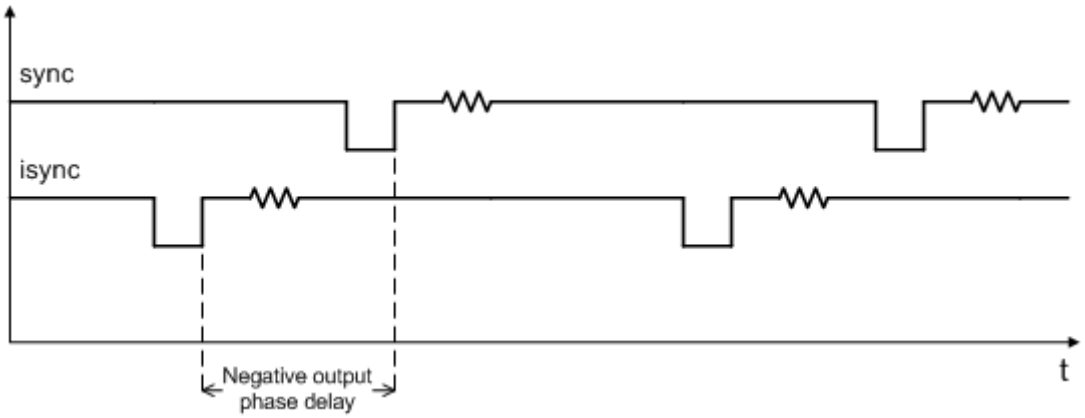


Figure 12: Negative phase delay

The *phase delay* can thus be written in several ways, a large positive delay will equal a small negative delay, because there is wrap-around on a frame basis. It follows that it is not useful to specify a *phase delay* larger than 1 frame. Strictly speaking the range could have been limited to -1/2 frame to 1/2 frame. For convenience, the delay range is allowed to be from -1 frame + 1100 samples to 1 frame – 1100 samples.

In order for FRS-HD-DMUX to honor the *phase delay* setting, it should ideally delay the incoming video between 0 to 1 frames. Because the processing delay through the card is 2 lines minimum, the actual window is between 2 lines and 1 frame + 2 lines. Hence, with the parameter (minimum) *video delay* set to 2 lines (the least number possible for the parameter); the output video will be between 2 lines and 1 frame + 2 lines delayed, with respect to the incoming video. A common occurrence in practical use is to synchronize an incoming video with a sync, but to let the outgoing video lead some samples or lines to the sync. This can easily be accomplished. Say that we want the outgoing video to occur 50 samples before the sync. We will then set the *phase delay* to -50 samples, and the *video delay* parameter to 2 lines. For convenience, let us assume that the incoming video is iso-synchronous, but that it lags 20 lines after the sync. We will then have the situation shown in Figure 13.

Note that the numbers in circles in the next figures are visualizing the video frames.

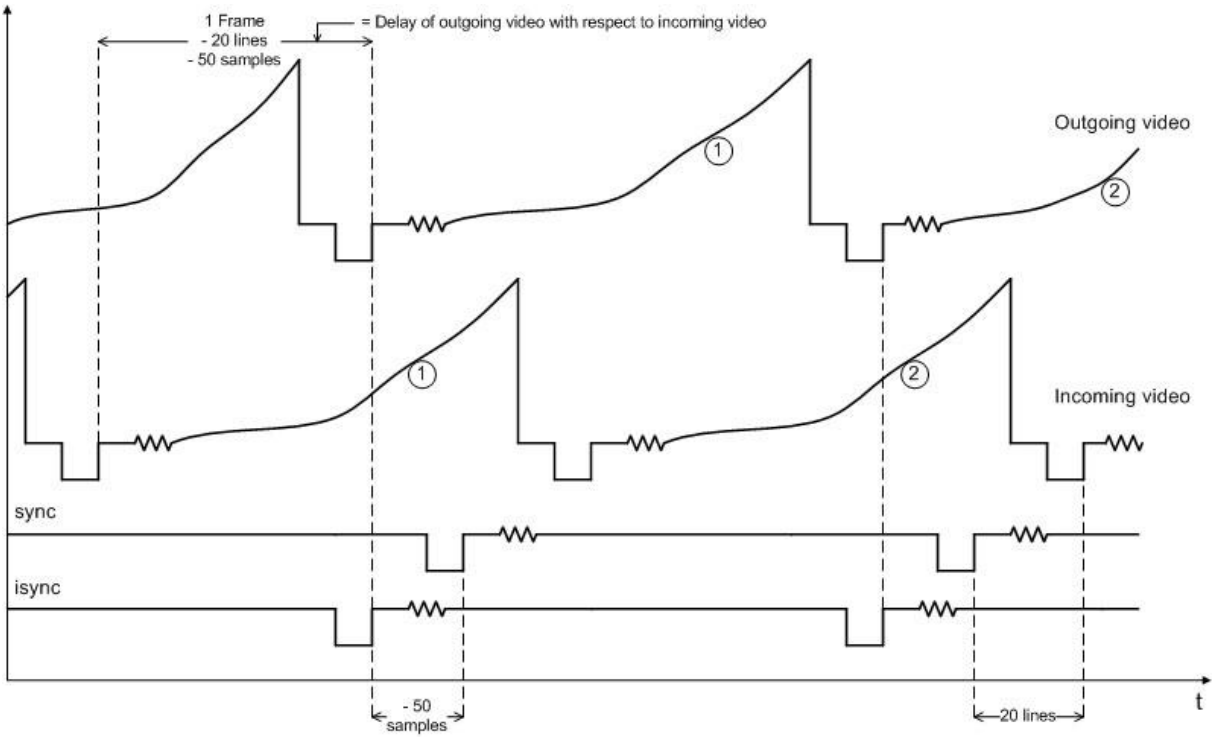


Figure 13: Example of delayed outgoing video

To match larger processing delays, one will want to first delay the incoming video, and then synchronize the video. This is equivalent to introducing a delay line for the incoming video, and then synchronizing the output of the delay line to the sync. In effect, one moves the delay-window start; this is equivalent with setting of the *video delay* to a larger value.

Let us assume that the *video delay* is set to 2 frames, 200 lines. In that case the outgoing video will be between 2 frames + 200 lines and 3 frames + 200 lines delayed with respect to the incoming video. For convenience, let us assume that the incoming video is iso-synchronous, but that it lags 25 lines after the sync. Let us also assume that the *phase delay* is set to -60 samples. We will then have the situation shown in Figure 14.

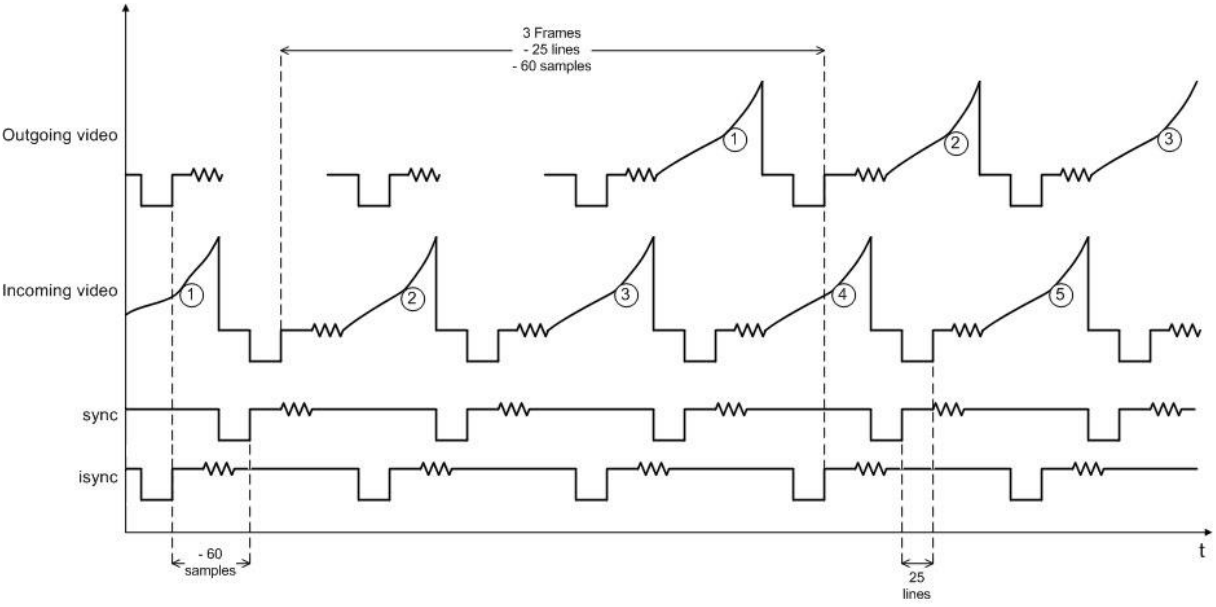


Figure 14: Another example of delayed outgoing video

To reiterate: The *phase delay* can be both positive and negative and sets the difference between the phase of the sync input and the video output. The *video delay* sets the delay between video output and video input. However, the actual delay might be longer as it also needs to phase up to the sync input. The actual delay may be up to 1 frame longer than the minimum video delay.

> The user may specify a *video delay* between 2 lines (min) and 7 frames (max).

The two parameters allow a user to delay the incoming video, and reference it to the sync input. By this mechanism, the user can precompensate processing delay in other equipment. The *video delay* setting simply determines a lower limit to a 1 frame wide window into a long delay line. The *phase delay* may be seen as a specification of the delay between the sync input, and a signal "isync". The output video is always synchronized to isync. A few more examples:

Example 1: The SDI input signal is isosynchronous to a sync signal, but 12 lines, 0 samples delayed. The *video delay* is set to 1 frame, 0 lines and 0 samples. The *phase delay* is set to 65 samples. The actual delay between the input video and the output video will be 2 frames - 12 lines + 65 samples.

Example 2: The SDI input signal is asynchronous to the sync signal (the frame frequency is slightly different). The *video delay* is set to 1 frame, 13 lines and 0 samples. The *phase delay* is set to -1 line. The actual delay will gradually change between 1 frame and 13 lines to 2 frames and 13 lines. The output will appear 1 line (in the output video format) ahead of the sync signal.

Example 3: The SDI input signal is isosynchronous to the sync signal, but 12 lines ahead of the sync signal. The *video delay* is set to 1 frame, 0 lines and 0 samples. The *phase delay* is set to -2 lines. The actual delay between the input video and the output video will be 1 frame + 10 lines.

The frames and lines are measured in units of the output SDI video standard. If the output SDI standard is 1080i25, a delay of one line is equal to 35.5us. If the output SDI standard is 720p50, a delay of one line is equal to 26.6us. If the output SDI standard is 625i25, a delay of one line is equal to 64us.

> For a scenario where the card receives different HD video standards, (e.g. 1080i25 and 720p50) the user may want to conserve a specific delay in microseconds for all HD video standards. This is accomplished by specifying the delay in number of samples instead of frames and lines. (For HD video standards the sample frequency is equal over standards, but the line and frame frequencies are different for the different standards).

If video input disappears

Given that stable SDI input and sync input exists: If the SDI input disappears, the picture will freeze for <*hold time*> and then go to video generator if the card is in default configuration.

When the SDI input disappears, the Frame Delay pulses at the back plane will also disappear.

If video input reappears

Given stable sync input, the video will reappear after <*lock time*> of locked video input if card is in default settings.

If sync input disappears

Given that stable SDI input and sync input exists: If the sync signal disappears, the card will act as in frame delay mode, see Chapter 5.5.2.

NOTE: This will result in a frame roll as the delay changes.

If sync input reappears

Given that a stable SDI input exists: If the sync signal reappears the delay mode will change back to Frame Sync mode. Hence the internal clock will be locked to the sync signal and the delay will again change.

NOTE: This will result in a frame roll as the delay changes.

If both signals disappears

The picture will first freeze for <*hold time*> and then go to video generator. The output is now referenced to the local clock source. However this clock source will be kept within 1 ppm of the last sync source.

5.5.2 Frame delay mode

In this mode a sync signal is not present. The delay set is then directly related to the incoming video. 1 frame and 1 line delay, means that the output will be 1 frame and 1 line delayed version of the input.

If video signal disappears

The picture will first freeze <*hold time*> and then go to video generator. The output is now referenced to the local clock source. However this clock source will be kept within 1 ppm of the last video source.

If video signal reappears

If the input video signal reappears, the video will reappear on the output <*lock time*> after stable input video. The delay will be set to the same delay as before loosing input.

NOTE: This may cause a frame roll.

If a sync input appears

Given that a stable SDI input exists: If a sync signal appears the delay mode will change to Frame Sync mode, see Chapter 5.5.1. Hence the internal clock will be locked to the sync signal and the delay will again change.

NOTE: This will result in a frame roll as the delay changes.

5.6 Video generator

The video generator can produce several simple signals: Color bar, Check field and flat field.

The flat field is possible to set up with 10bit (0-1023) luma and chroma values, or by selecting a color.

The generator may be used as the video source if there is no video signal present at either of the video inputs. The generator may also be switched on with Gyda. This will override video input but the generator signal will be locked to the input.

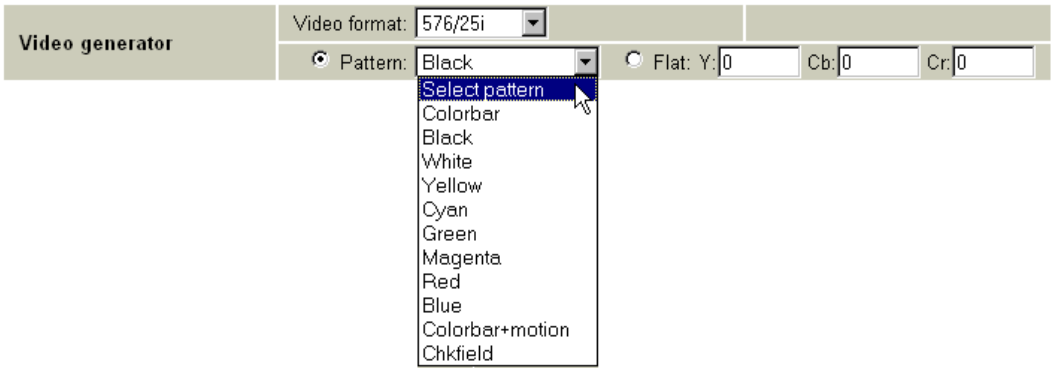


Figure 15: Gyda view of the video generator

5.7 Label generator

The label generator consist of 2 lines of 16 characters each that are placed at the lower left corner of the active area.

Its main function enables the user to automatically add a label to the internal generator at loss of input signal. It is done by selecting the auto tick-box on the “Label gen” block in the Gyda configuration.

It is also possible to insert the label to the incoming SDI by ticking on the “On” tick-box.

> Note that to see the label on an output the video output selection must be set to “processed” for this specific output.

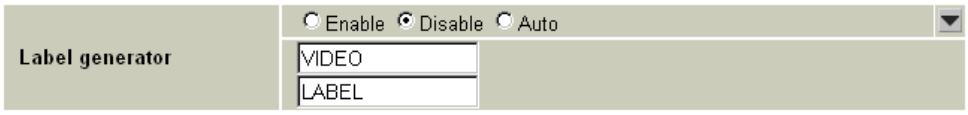


Figure 16: Gyda view of label generator

5.8 Video processing block

The video processing block consists of a *gain and offset* adjustment, and a video payload *legalizer*.

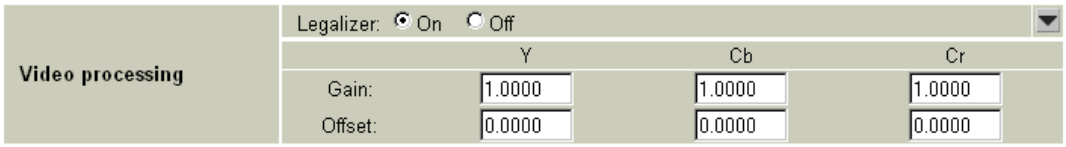


Figure 17: Gyda view of the video processing block

5.8.1 Gain and offset

The gain and offset adjustment is done separately on the Y, Cb and Cr samples.

	Range in Multicon Gyda
Luma gain	0 – 4x
Chroma gain	0 – 4x
Luma offset (gain =1)	-511.75 – 511.75 (in sample values)
Chroma offset (gain = 1)	-255.75 – 255.75 (in sample values)

5.8.2 Video payload legalizer

The legalizer hard clips the upper and lower limit of the video payload. With the legalizer enabled these limits are:

Upper limit	Luma:	3ACh
	Chroma:	3C0h
Lower limit	Luma:	040h
	Chroma:	040h

With the legalizer disabled, the video processing block hard clips both luma and chroma to 3FBh and 004h.

> Note that the payload legalizer gives out a trigger to the video content trigger block when output has been clipped.

5.9 EDH processing block

If enabled, the EDH processing block extracts the EDH package from the video, updates the EDH flags according to SMPTE RP165 and inserts the EDH package into the ancillary data of the video.

If disabled, The EDH processing block only reads, process and report the EDH package without changing it in video stream.

5.10 Video output selection

The board has four outputs where two and two can be either routed directly from the re-clocker or routed through the processing unit.

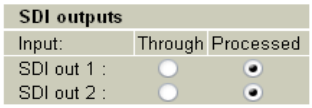


Figure 18: Gyda view of SDI output selection block

When processed is selected, it is possible to either output video generator or mute the output. This is done at the *video in - mode* by selecting *Video gen.* or *Mute*. This will not have any effect on outputs set in through mode.

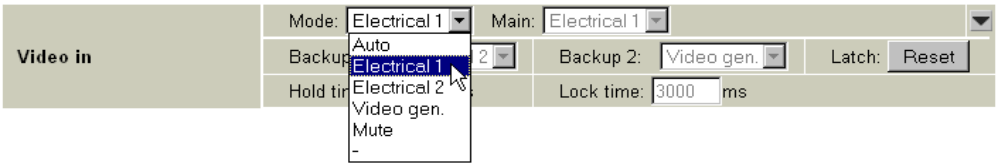


Figure 19: Gyda view of video input mode.

5.11 Audio blocks overview

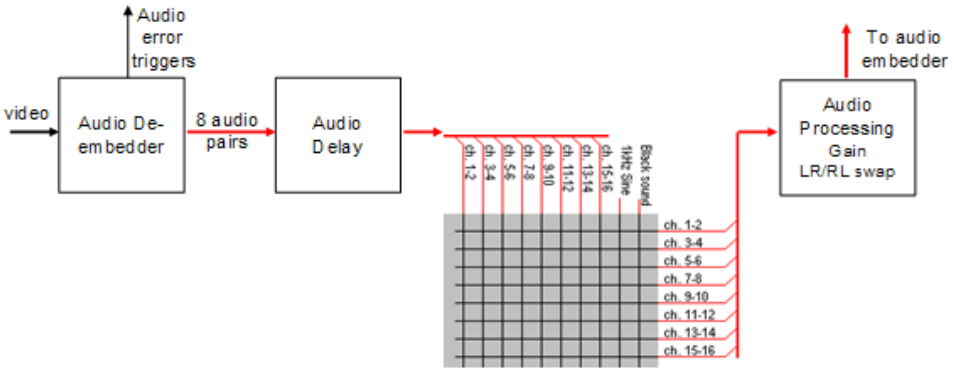


Figure 20: Audio function blocks

5.12 Audio de-embedder

The Audio de-embedder extracts all audio embedded in the video stream. The de-embedder is always enabled.

5.13 Audio delay

An audio delay relative to the video output can be specified commonly for all de-embedded channels. This is done in Gyda. The audio delay is specified in audio samples relative to the output video, and can be both positive and negative.

> Note that as the audio delay is relative to the video output it is possible to specify an audio delay that will be an actual negative delay. This will cause audio errors.

The *negative* audio delay is limited by the *positive* video delay. Since the audio delay is always relative to the video, the only way to give the audio a negative delay is to delay the video by a positive amount. To go beyond this limit would require the audio to be re-embedded before it had even been de-embedded from the incoming video, and that is of course impossible.

The positive audio delay is limited by the fact that the sum of the video delay and the relative audio delay cannot be larger than 32000 audio samples (approx. 0.67 ms with 48 kHz audio). If the video delay is set to minimum, the full 32000 audio samples will be available, but if the video delay is set to – say – 5 frames, the maximum relative audio delay is reduced to 20000 audio samples (assuming 25 frames per second, 5 frames equals 0.2 seconds, which in turn equals 12000 audio samples, and 32000-12000=20000). When doing these calculations, remember that if a sync reference is present, a video delay setting of N frames means that the actual video delay can vary continuously between N and (N+1) frames. The calculations should therefore be based on (N+1) frames.

Dolby-E delay handling

The FRS-HD-CHO can re-align Dolby-E with video. Dolby-E processing equipment typically causes one frame delay for the audio.

The positive *video delay* needs to be set higher than the desired negative relative audio delay. Then set a negative relative audio delay that corresponds to a whole number of full frames of audio samples[6]. A delay example setting is shown in Figure 21. The audio embedder settings should be as in Figure 22.

Phase delay	0	lines	0	samples		
Video delay	2	frames	0	lines	0	samples
Relative audio delay	-960	samples				

Figure 21: Gyda view of the delay settings. The video is delayed 1 frames compared with the audio for a 50Hz signal.

Audio embedder bypass	○ Enable	◉ Disable						
Audio emb. ch 1-4	◉ Enable	○ Disable	Acp:	◉ On	○ Off	◉ 24 bit	○ 20 bit	
Audio emb. ch 5-8	◉ Enable	○ Disable	Acp:	◉ On	○ Off	◉ 24 bit	○ 20 bit	
Audio emb. ch 9-12	◉ Enable	○ Disable	Acp:	◉ On	○ Off	◉ 24 bit	○ 20 bit	
Audio emb. ch 13-16	◉ Enable	○ Disable	Acp:	◉ On	○ Off	◉ 24 bit	○ 20 bit	

Figure 22: Gyda view of the audio embedder settings

[6] To calculate number of audio samples/frame simply divide 48000 with frame rate (24Hz, 25Hz, 29.97Hz, 30Hz, 50Hz, 59.94Hz or 60Hz)

5.14 Audio cross point matrix

The audio cross point matrix is an 8x10 cross point with inputs and outputs as shown in Figure 20. The 8 de-embedded channels, a 1 kHz sine and “black sound” are selectable inputs. “Black sound” is explained in Chapter 5.2. The outputs of the cross points are 8 stereo channels for re-embedding.

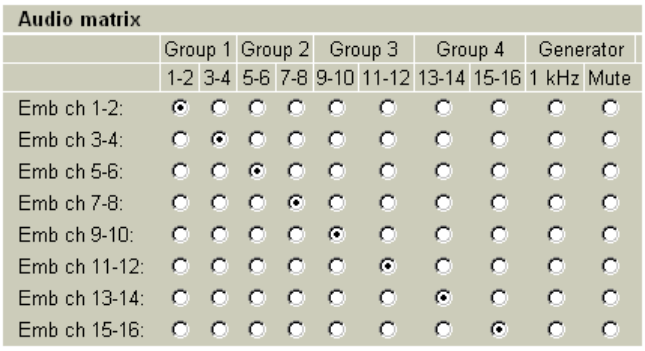


Figure 23: Gyda configuration view of the audio cross point matrix

All outputs have a common fallback option that can be set in Gyda. The priorities can be selected between *matrix* (being the choice in the cross point matrix), *sine, mute or delete. Mute* is merely silence, while *Delete* deletes any audio content and set the audio control package to channel delete for its respective channels.

5.15 Audio generator

The stereo audio generator is available in the audio cross point matrix as a source. It is a high purity 1 kHz sine wave with a 250ms interruption on the left channel every 3 seconds. The audio level may be set to one of two standards. The two levels are -18 dBFS and -20 dBFS. These two levels correspond to EBU R68 and SMPTE RP 155.

5.16 Audio processing block

The output of each stereo signal from the audio cross point matrix may be processed in the audio processing block. This is controlled with the Gyda controller. The processing includes channel L/R manipulation and audio gain.

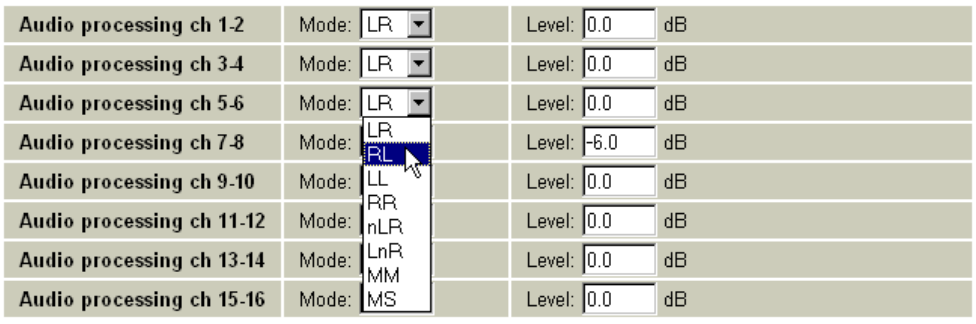


Figure 24: The figure shows the Gyda configuration view of the audio processing block

Channel L/R manipulation

The stereo signals may be output in one of the following ways:

- LR, Left / Right	No change.
- RL, Right/ Left	Channels are swapped.
- LL, Left/ Left	Left channel is copied into the right channel.
- RR, Right/ Right	Right channel is copied into the left channel.
- nLR, ØLeft/ Right	The left channel is phase inverted.
- LnR, Left/ ØRight	The right channel is phase inverted.
- MM, (Left + Right)/2	The left and right channels are summed.
- MS, MS/AB	The left and right channels are converted from AB stereo to MS stereo.

The sum products (L+R/2 and MS) are reduced in level by 6 dB to avoid any possibility of clipping.

Audio gain

Audio gain is a 16 bit value that can be set for each stereo pair going into the audio processing block. The actual gain is the 16bit value/ 100dB. The gain range is set to [+96dB, -96dB] with a gain step of 0.1dB.

> Note that non-audio data is ignored and left unchanged by the gain function.

5.17 Audio embedder

Audio emb. ch 1-4	◉ Enable	○ Disable	Acp:	◉ On	○ Off	◉ 24 bit	○ 20 bit
Audio emb. ch 5-8	◉ Enable	○ Disable	Acp:	◉ On	○ Off	◉ 24 bit	○ 20 bit
Audio emb. ch 9-12	◉ Enable	○ Disable	Acp:	◉ On	○ Off	◉ 24 bit	○ 20 bit
Audio emb. ch 13-16	◉ Enable	○ Disable	Acp:	◉ On	○ Off	◉ 24 bit	○ 20 bit

Figure 25: Gyda view of the audio embedders

The audio embedder can be enabled per group in Gyda. When a group is disabled the audio inside that group is removed.

When in SD mode, a 24bit sound signal can be changed to 20bit through Gyda control. This removes the upper 4 bits of the signal. The audio control package is left unchanged as the bit range is still present.

The audio control package can also be switched on and off in SD mode through Gyda control.

The audio embedder can be switched off all together. In this state the audio embedded on the input signal is left unchanged.

6 RS422 commands

6.1 FLP4.0 required commands

Block	Blk#	Commands	Example	Response	Control
-	-	?	?	*product name*\ SW rev *n.m*\ FW rev *r.s*\ protocol ver 4.0\	***Hello* command**. *Note 1: No other commands will be available until the card has received this hello.* *Note 2: This command will also enable checksums.* *Note 3: Cards are designed to be hot-swappable. To sync with the start of a new command, the cards will wait for a <lf> character before looking for a valid command.*
conf	0	-	conf 0	*too long to list*	**Configuration settings** Retrieves the card's configurable settings. Each addressable block is represented by a single line. Dynamic status *may* be included in response, but is usually reported in *info* only.
-	-	info	info	*too long to list*	**Dynamic status info** Blocks with static settings only will usually not be included, see *conf* above.
-	-	chk off	chk off	ok	**Checksum off** If issued twice in succession, this command will disable checksums. Note: Responses will still have the checksums appended. *NOTE1: ? command turns the checksum back on*
-	-	locate on <seconds> locate off	locate on 3 locate off	ok	**Card locator** This command will cause all the LEDs to flash for a user specified number of seconds. If omitted, the value <seconds> will be set to a default of 120 seconds. The flashing can be terminated at any time with *locate off*.
-	-	address	address	address <address>	**Card address** This command will check and update the card's current rack and slot address, which is normally only done at start-up.
-	-	filename	filename frshdcho-0-105.ffw filename frshdcho-0-100.mfw	<name>'.'<extension>	**Firmware upgrades** The <name> part must match the card's hardware and include a revision number, and the extension must be either 'ffw' for FPGA firmware or 'mfw' for microcontroller firmware. After running this command the board will wait for the firmware in Intel-hex format.

-	-	fin	fin	ok	**Finalize** Finalize the programming of the microcontroller. See description of the uC bootloader (separate document).
misc	0	-	NOT AVAILABLE BY COMMAND. ONLY FOUND in Conf 0	prog | fin ' ' | ovr	**Misc info** *prog* if the card is freshly programmed by the bootloader and the program is still un-finalized. *fin* is the normal condition. *ovr* if DIP-switch 16 is set to the ON position and the card is under DIP-switch control. Note 1: The info part of misc has additional functionality when locate is used: *locating <remaining seconds>.* This enables a visible countdown clock in Gyda, but is not a required part of FLP400.

6.2 Normal control blocks

Block	Blk #	Commands	Example	Response	Control
ceq	0	-	ceq 0	cd | ncd	cable equalizer for electrical input 1. No control, only used to report *carry detect* or *not carry detect.*
ceq	1	-	ceq 0	cd | ncd	cable equalizer for electrical input 2. No control, only used to report *carry detect* or *not carry detect.*
cho	0	pri <k> | pri <k> <l> | pri <k> <l> <m> pos man <k> | pos auto latch reset t1 <hold_time> t2 <lock_time>	cho 0 pri 0 cho pri 0 1 cho pri 10 2 cho 0 pos man 1 cho 0 pos auto cho 0 latch reset cho 0 t1 1000 cho 0 t2 1000	size 5 pri *k*,*l*,*m* auto t1 <hold time> t2 <lock time> size 5 pri *k*,*l*,*m* man *m* t1 <hold time> t2 <lock time>	**Video input select** ***pri*:** a prioritized list of inputs, used when change-over is automatic. The list can have 1, 2 or 3 entries, or *levels*. Manual mode is effectively the same as automatic mode with one priority level only, but has its own command. 0 = from electrical input 1 1 = from electrical input 2 2 = mute 3 = internal video generator 4 = none The module will always respond with 3 levels, filling in 4=none for the levels not used. ***t1* and *t2*:** change-over doesn't happen immediately, as a precaution against glitches and unstable signals. The timers t1 and t2 let the user decide how long (in ms) we will cling on to a missing input before we consider it gone and move on to the next pri level, and how long an input with a higher priority should be present before we consider it repaired and switch back, respectively. Note: MCU firmware before ver. 1.10 also have latch and rule settings. These are deprecated.

cho	1			size 3 pri *k*,*l* auto size 3 pri *k*,*l* man *m*	No commands available. Included to show internal status and to update Gyda graphics.
cho	2-9	pri <k> | pri <k> <l>	cho 2 pri 1 cho 5 pri 0 2	size 4 pri *k*,*l*	**Audio fallback setting** Audio change-over blocks, one cho per audio output from the audio matrix, mtx 0. No other settings but the priority list. 0 = from audio matrix 1 = sine 2 = black sound 3 = mute *Note: Only generators (pri 1, 2 or 3) are allowed to be set as first and only priority.*
cho	10	pri <k> | pri <k> <l>	cho 12 pri 1 cho 12 pri 0 2	size 4 pri *k*,*l*	**Audio common fallback setting** A short-cut to set change-overs 2-11 all at once. Will of course not report anything in info, that's left to the individual cho blocks.
gpi	0	act | inact	gpi 0 act gpi 0 inact		**EDH insert select** This gpi works as a simple 2:1 switch. inact : EDH off act : EDH on
gpi	1	act | inact	gpi 1 act gpi 1 inact		**GPO compatibility modus** This gpi works as a simple 2:1 switch. inact: GPOs are pin compatible with the FRS-HD-DMUX range act: GPOs are pin compatible with the earlier SDI-CHO-2X1 range
gpi	2	act | inact	gpi 1 act gpi 1 inact		**Input signal type (Available from MCU firmware 1.10, and then only for FRS-HD-CHO-ASI, i.e. if the optional ASI functionality has been purchased)** This gpi works as a simple 2:1 switch. inact: The module expects SDI input and behaves just like the FRS-HD-CHO. act: The module expects ASI input. SDI input will still be accepted, but all SDI processing blocks will be bypassed.
rcl	0	-	rcl 0	lock | lol	Reclocker. No control, only used to report *lock status.*
emb	0-3	en | dis acp (on | off) use24 (on | off) del (off | (on <del12> <del34>))	emb 0 en emb 2 dis emb 1 acp on emb 3 acp off emb 1 use24 on emb 2 use24 off emb 0 del off emb 2 del on 54 -432	(en | dis) use24 (on | off) acp (on | off) del (off | (on <del12> <del34>))	**Audio embedder block** **en/dis:** Enables or disables the embedding of the group into the ancillary area. **acp on/off:** This is valid only for SD and enables the audio control package. **use24 on/off:** This is only valid for SD and selects between 24bit and 20bit sound. **del off/on delay12 delay34:** For each of the embedder groups the delay bits for ch1+2 and for ch3+4 can be inserted into the ACP. The delay value can be positive and negative and is put directly into the ACP as it is written. *Note: To set both delays to 0 would be the same as turning the delays off. The response reflects this.*

demb	0-3	-	demb 0 demb 2	grp *k* en	**Audio de-embedders** one permanently assigned to each incoming group, always enabled. No control available.
vprc	0	lglz on | lglz off (y | cb | cr) <gain> <offset>	vprc 0 lglz on vprc 0 lglz off vprc 0 y 8192 0 vprc 0 cb 2000 0 vprc 0 cr 1000 1000		**Video processing block** Gain and offset are both signed fixed point numbers. Gain is in 2.13-format, while offset for Y and the chroma channels are given in 10.2 and 9.2 respectively. Gain range is 0 – 32767, $Gain_{=0x}$ = 0, $Gain_{=1x}$ = 8192, $Gain_{=4x}$ = 32767 Luma Offset range is -4095 – 4095, $Offset_{=0}$ = 0 Chroma Offset range is -2047 – 2047, $Offset_{=0}$ = 0
sync	0	-	sync 0	'lol' | ('lock' ('trilvl' | 'bb' | 'sdi'))	Frequency reference for video output. Status only, no commands available.
dly	0	<frames>frms <lines>lines <samples>sps	dly 0 2frms dly 0 2lines 30sps dly 0 0frms 50sps dly 0 0frms 3lines 50sps	'tgt' <frames> frms <lines> lines <samples> sps	**Video delay** This sets the minimum video delay of the card. In info this block reports back the current delay in nanoseconds. This will vary with the incoming video standard.
dly	1	<audio_samples>sps	dly 1 -30sps	'tgt' <audio_samples> sps	**audio delay** The audio delay is given in audio samples. Audio delay is always given relative to video.
dly	2	<lines>lines <samples>sps	dly 2 1lines -30sps	'phase' <lines> lines <samples> sps	**Video phase** If lines != 0 the resulting phase will vary with incoming video standard, see dly 0 above.
vgen	0	cbar | chkfield | white | yellow | cyan | green | magenta | red | blue | black flat <Y> <Cb> <Cr> video <lns>/<rate><scan> wss (auto|off | (on <wss_val>))	vgen 0 cbar vgen 0 flat 200 0 100 vgen 0 video 1080/24p vgen 0 video 1080/25p vgen 0 video 1080/25i vgen 0 video 1080/29i vgen 0 video 1080/30i vgen 0 video 720/24p vgen 0 video 720/25p vgen 0 video 720/29p vgen 0 video 720/30p vgen 0 wss auto vgen 0 wss on 7	video <lns>/<rate><scan> wss (auto| off | (on <wss_value>)) (cbar | chkfield | white | yellow | cyan | green | magenta | red | blue | black | (flat <Y> <Cb> <Cr>))	**Internal video generator.** The video generator will be activated in two different ways: If selected as a fallback option the generator will generate the selected pattern when the other input(s) are missing, and then use the video settings from the last external source present. It can also be selected as the main input in cho 1, in which case its own video settings will also be used.
edh	0	msk <24b_mask> reset	edh 0 msk 0xFE0005 edh 0 reset	msk <24b_mask>	**Error detection and handling** Error counting. The count itself is reported in info. Errors can be masked off and not counted; this is the purpose of the mask. The counter itself is 16b and will wrap around, but can also be reset by issuing *reset*.

mtx	0	<i1> <o1> ...<iN> <oN> <i1> <o1>,<o2>,...<oN> <i1> <o1> - <o2> ..or the above combined	mtx 0 0 2 1 4 5 5 mtx 0 0 0, 1 1, 2 2 mtx 0 0 0-9 mtx 0 0 0 1 1 2 2-7	size M:N i1 i2 i3... iN	**Audio matrix** mtx 0 (size 10:8) controls the audio matrix; outputs 0-7 are embedded sound; inputs 0-7 are de-embedded audio, 8=1kHz sine, 9=Black/silence *Note: Any combination of the three basic commands are allowed, for instance the following command to set up a 10x10 audio matrix in a single line:* *mtx 0 1 1 2 2 3 0,3-7* *=> mtx 0 size 10:10 3 1 2 3 3 3 3 3 3*
mtx	1	<i1> <o1> ...<i2> <o2> <i1> <o1>,<o2>	mtx 1 0 0 1 1 mtx 1 0 0,1	size M:N i1 i2 i3... iN	**Video output matrix** mtx 1 (size 2:2) controls the video output switches. 0: Through mode (re-clocked only) 1: Processed mode (SDI from FPGA
mtx	2	<i1> <o1>	mtx 2 0 0 mtx 2 1 0	size M:N i1 i2 i3... iN	**Audio embedder bypass** 0: Embedding disabled 1: Embedding enabled
agen	0	lvl <sine_level>cBFS	agen lvl -180 agen lvl -200	sine 1kHz lvl <sine_level>cBFS	**Audio generator** The amplitude of the generated sine that can be chosen as fallback in audio change-overs. Legal values are -180cBFS or -200cBFS (centiBel referred to full scale output). Units are optional, but if included must be written as cBFS (case sensitive).
aprc	0-9	lr | rl | ll | rr | nlr | lnr | mm | ms | lvl <gain>	aprc 0 lr aprc 3 ll aprc 6 mm aprc 7 lvl -400	lr | rl | ll | rr | nlr | lnr | mm | ms	**Audio processing** one block for each output from cho 2-9 that is routed to the embedder. The meaning of the commands are as follows: lr = Normal rl = Channel swapped ll = Left channel to both output channels rr = Right channel to both output channels nlr = Left channel phase inverted lnr = Right channel phase inverted mm = Mono, both channels = (r+l)/2 ms = Mono/stereo, m=(l+r)/2, s=(l-r)/2 lvl means level and is the gain setting.
trig	0-8	msk <mask> ('&' | '|') en | dis t1 <hold_time> lvl <bitnr> <threshold>	trig 3 msk 0x13 | trig 0 dis trig 2 t1 1000 trig 6 lvl 0 -65	en msk 0x0 | t1 0x2710 lvl 0 -66	**Triggers for synchronous switching** The trig blocks responsible for the synchronous switching between the electrical inputs. Each trig block has it's own hold time and a mask that select which bits should be taken into account, and if these bits should be or'ed or and'ed together. Some bits may have a user selectable threshold values. In the case that one threshold is valid for several bits, the lowest bit number is used. For instance, silence threshold in 'Audio in silence trigger' is valid for all 8 bits, but the command targets bit 0 only. For bit masks, see chapter 5.3 on input selection and triggers.
supr	0	en | dis | auto lb <page> <L1> <L2>…<L16> font <tag>	supr 0 auto supr 0 lbl 0 65 66 67 0 supr 0 font 1252	Supr 0 en font 0x4e4 lb 0 86 73 68 69 79 10 76 65 66 69 76	**Label generator** A label generator can be superimposed on the video. The setting 'en' means it is always superimposed, 'dis' means it is

					never superimposed, and 'auto' means it is superimposed on the internal video generator only. The text in the label can be set or modified by the lb <page> sub-command, where page is 0 to operate on letters 1-16 or 1 to operate on the letters 17-32. The letters follow as a string of ASCII numbers. To write more than 16 letters, two commands must be issued. A string is always terminated at an ASCII 0, and ASCII 10 is linefeed/new line. Only the first ASCII 10 will be honored. In the second example command, the label string is set to 'ABC' and terminated with ASCII 0. If not terminated, the command would've modified the first 3 letters of the string, but any remains of a previous string would still be present (until ASCII 0 or 33rd letter encountered). *Note 1: When the flash is busy programming the FPGA or is being programmed with new FPGA code, label information can not be updated.* *Note 2: At the present, only one font/codepage (codepage 1252) is included in the module.*

6.3 Commands intended for debug/lab use only

Block	Blk#	Commands	example	Response	Control
spi	-	on | off	spi on spi off		spi off used to isolate the uC from the SPI lines during programming of the flash by external programmer. spi on must be issued in order to re-enable normal card operation with the uC as the SPI master.
spir	-	<address>	spir 0x0004		Read a single word (or byte) from a SPI registers. Addressing is 16b and most significant nibble determines which chip. These are the address ranges: 0x0000 – 0x0fff : Reserved audio DAC, not present in FRS-HD-CHO 0x1000 – 0x1fff : FPGA 0x2000 – 0x2fff : flash 0x3000 – 0x3fff : deserializer 0x4000 – 0x4fff : serializer 0x5000 – 0x5fff : shift register (for LEDs)
spiw	-	<address> <data>	spiw 0x0004 0x2c		With the same address ranges as for spir above, this command allows the user to modify SPI registers.
thebug	-	-	thebug		A collection of debug information that is presented in a Gyda block-like format. First line tells which image is currently loaded. Second line contains the filename and version of the uC software, including the AVR controller it was compiled for. The third line contains the SW flags in uC, the number of times the watchdog timer has kicked in, readout of dip-switches, input select for deserializer, SDOn on/off, slew rates, and status for the video changeovers. The next two lines contain raster information from the deserializer and serializer respectively, while the next two lines contain sample values for mlines and VCXO.

General environmental requirements for Nevion equipment

1. The equipment will meet the guaranteed performance specification under the following environmental conditions:
   - Operating room temperature range: 0°C to 45°C
   - Operating relative humidity range: <90% (non-condensing)

2. The equipment will operate without damage under the following environmental conditions:
   - Temperature range: -10°C to 55°C
   - Relative humidity range: <95% (non-condensing)

Product Warranty

The warranty terms and conditions for the product(s) covered by this manual follow the General Sales Conditions by Nevion, which are available on the company web site:

www.nevion.com

Appendix A Materials declaration and recycling information

A.1 Materials declaration

For product sold into China after 1st March 2007, we comply with the “Administrative Measure on the Control of Pollution by Electronic Information Products”. In the first stage of this legislation, content of six hazardous materials has to be declared. The table below shows the required information.

組成名稱 Part Name	Toxic or hazardous substances and elements					
	鉛 Lead (Pb)	汞 Mercury (Hg)	镉 Cadmium (Cd)	六价铬 Hexavalent Chromium (Cr(VI))	多溴联苯 Polybrominated biphenyls (PBB)	多溴二苯醚 Polybrominated diphenyl ethers (PBDE)
FRS-HD-CHO/ FRS-HD-CHO-ASI ASI-CHO-2x1-PB	O	O	O	O	O	O
O: Indicates that this toxic or hazardous substance contained in all of the homogeneous materials for this part is below the limit requirement in SJ/T11363-2006. X: Indicates that this toxic or hazardous substance contained in at least one of the homogeneous materials used for this part is above the limit requirement in SJ/T11363-2006.						

This is indicated by the product marking:

A.2 Recycling information

Nevion provides assistance to customers and recyclers through our web site http://www.nevion.com/. Please contact Nevion Customer Support for assistance with recycling if this site does not show the information you require.

Where it is not possible to return the product to Nevion or its agents for recycling, the following general information may be of assistance:

- Before attempting disassembly, ensure the product is completely disconnected from power and signal connections.
- All major parts are marked or labeled to show their material content.
- Depending on the date of manufacture, this product may contain lead in solder.

Some circuit boards may contain battery-backed memory devices.